

HIGH RELIABILITY MEMORY SUBSYSTEM USING DATA ERROR CORRECTING CODE SYMBOL SLICED COMMAND REPOWERING

ABSTRACT OF THE DISCLOSURE

A memory subsystem comprising: a command register in operable communication with a plurality of memory devices via a plurality of command buses. The plurality of memory devices is arranged into symbol slices and each symbol slice is configured to be part of a single error correction code packet. Each command bus of the plurality of command buses is configured to interface between the command register and each memory device in a particular symbol slice. A method of command bus redundancy comprising: configuring a plurality of memory devices into symbol slices, each symbol slice configured to be part of a single error correction code packet; establishing a plurality of command buses, each command bus configured to interface with each memory device in a particular symbol slice; and configuring a command register with sufficient command bus drivers to support each command bus of the plurality of command buses.